# Liang-Kai Wang

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**Objective**

A full-time research and/or development position in the areas of computer architecture, computer arithmetic, processor and ASIC design, or VLSI systems.

**Experience**

**Qualcomm, Austin, TX**

September 2010 ~ Present

RTL design, implementation, and verification for Qualcomm Hexagon DSP Combined Integer and Floating-point Unit.

Major responsibility:

1. RTL design for **760** arithmetic instructions, including
   1. Single and double precision add/sub/multiply/Fuse-Multiply Add (**FMA**) unit.
   2. Format conversion between integer and floating-point and between single and double precision floating point number.
   3. Divide and square root helper functions
   4. Integer instructions, which include normal binary add, sub with saturation, rounding, as well as vector arithmetic
2. Work with verification team to develop test coverage for floating point operations.
3. Work with physical design team to develop placement and routing strategy for multiplier

**First author for the paper published in QTech 2011 (internal conference, 3rd place of the entire hardware section)**

**AMD, Austin, TX**

August 2007 ~ September 2010

1. Design and Implementation of AMD 28nm processor core. Integer Unit/Bypass Network (2010).
2. Design and Implementation of AMD 32nm processor core, Instruction Fetch/Cache unit, [Llano](http://www.semiaccurate.com/2010/02/10/amd-finally-outs-32nm-llano-core/). (2009)
3. Design and Implementation of AMD 32nm processor core, Floatong-point unit, [Bulldozer](http://en.wikipedia.org/wiki/Bulldozer_(processor)) (2009)
4. Design and Implementation of AMD [Bobcat](http://en.wikipedia.org/wiki/Bobcat_(processor)) core, Floating-point unit (2007)

Major role in all projects:

Major responsibilities include logic design and synthesis, timing convergence, floorplanning, logical equivalence checking, design placement and routing, noise analysis, electrical analysis, etc.

**Reference**: one available on LinkedIn. Others upon requests.

**Intel, Folsom, CA, DFT Co-op engineer**

June 2004 – January 2005

Developed a Random Instruction Test (RIT) generation tool for Intel’s cellular and application processors to run on-chip functional testing.

**Experience (continued)**

**Research Assistant, UW-Madison**

January 2003 – August 2007 (Supervisor: Dr. Michael J. Schulte)

##### Developed and evaluated novel algorithms for decimal arithmetic

**Teaching Assistant for graduate level course, VLSI Design and Digital Circuits, UW-Madison**

January 2004 ~ May 2004 (Supervisor: Mr. Eric Hoffman)

##### Teaching assistant for the undergraduate/graduate course, Digital Circuits and Components

##### **Research Assistant in VLSI Design, UW-Madison**

##### September 2002 ~ January 2003 (Advisor: Professor Charlie Chen)

Designed and evaluated a high-speed adder.

**Lieutenant in Coast Guard Administration, Central Coastal Patrol Office**

July 1999 ~ May 2001

Led a company of about 100 soldiers and responsible for patrolling the territory waters, apprehending smugglers, and carrying out rescue operations.

Help manage transition of the office from the original maritime patrol agency

**Education**

**Ph.D.** **in** **Electrical and Computer Engineering,** Aug 2007

University of Wisconsin-Madison.

**Thesis -** Processor Support for Decimal Floating-Point Arithmetic

**Advisor** - Professor Michael J. Schulte

**Dissertation Committee**

- Prof. Yu Hen Hu, Prof.Mikko H. Lipasti, Prof. Kewal K. Saluja, and Prof.David A. Wood

**M.S. in Electrical and Computer Engineering,** December 2003

University of Wisconsin – Madison. Major in Computer Architecture and VLSI Design

**B.S. in Electronic Engineering,** June 1999

National Chiao Tung University, Hsinchu, Taiwan.

**Specialty and Annual Review**

Expertise in computer arithmetic and design. Very knowledgeable in both high performance and low power designs, especially the arithmetic logic (both integer and floating-point), data bypassing, and cache way prediction. Extensive logic design experience in arithmetic circuits and instruction fetch unit in both 32-nanometer and next generation processor core.

Top in the team 2009 Annual and 2010 Midyear performance review (AMD). (3 being the highest in both categories)

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| **POTENTIAL:** | 3.0 - High Potential |
| **PERFORMANCE:** | 3.0 - Exceeding Expectations |

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| **Patents, Awards, Talks, and Publications: Total 13 publications** |
| 1. L.-K. Wang, S. Balasubramanian, “Design Challenges of Unified Floating Point and Integer Unit with Fused Multiply Accumulate in QDSP6 Core”, **QTECH** (Qualcomm Internal Conference) June 14, **2011** (**3rd place** of entire hardware section)  2. L.-K. Wang, M. A. Erle, C. Tsen, E. M. Schwarz, and M. J. Schulte, “A Survey of Hardware Designs for Decimal Arithmetic”, ***IBM*** *Journal of Research and Development*, vol 54, no. 2, **2010**. |
| 3. M. J. Anderson, C. Tsen, L.-K. Wang, K. Compton, M. J. Schulte, “Performance Analysis of Decimal Floating-Point Libraries and Its Impact on Decimal Hardware and Software Solutions”, IEEE International Conference on Computer Design (ICCD), 2009 |
| 4. L.-K. Wang and Michael J. Schulte, “A Decimal Floating-Point Adder with Decoded Operands and a Decimal Leading-Zero Anticipator”, IEEE Symposium on Computer Arithmetic, June 2009 |
| 5. L.-K. Wang, Michael J. Schulte, John D. Thompson, and Nandini Jairam, “Hardware Designs for Decimal Floating-Point Addition and Related Operations”, IEEE Transactions on Computers, March 2009 |
| 6. L.-K. Wang, “Designs of Decimal Leading Zero Detector and Anticipator for High Speed Decimal Floating-point Arithmetic”, US Patent Application, Liang-Kai Wang, 2009 |
| 7. L.-K. Wang and M. J. Schulte, “Processing Unit Having Decimal Floating-Point Divider Using Newton-Raphson Iteration," United States Patent 7,467,174, Dec. 2008 |
| 8. L.-K. Wang, C. Tsen, D. Jhalani, and M. J. Schulte, “Benchmarks and Performance Analysis for Decimal Floating-point Applications”, IEEE ICCD, October 2007 (**Best Paper Award**) |
| 9. L.-K. Wang and M. J. Schulte, “Decimal Floating-Point Divider Using Newton-Raphson Iteration”, in Journal of VLSI Signal Processing Systems (Featuring the **Best Papers** from ASAP2004), October 2007. |
| 10. L.-K. Wang, J. D. Thompson, N. Karra and M. J. Schulte, “Hardware Design for Decimal Floating-point Addition and Related Operations”, IEEE Transaction on Computers, Aug 2007 |
| 11. L.-K. Wang and M. J. Schulte, “Decimal Floating-Point Adder and Multi-function Unit with Injection-Based Rounding”, IEEE Symposium on Computer Arithmetic, June, 2007 |
| 12. L.-K. Wang and M.. J. Schulte, “Decimal Floating-Point Square Root Using Newton-Raphson Iteration”, IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP), July, 2005 |
| 13. L.-K. Wang and M. J. Schulte, “Decimal Floating-Point Division Using Newton-Raphson Iteration”, IEEE ASAP, September, 2004  14. L.-K. Wang, “An Introduction to Computer Arithmetic”, Talk at National Chiao Tung University, Department of Electronics Engineer, 2011  15. L.-K. Wang, “An Introduction to Computer Arithmetic and Others”, Seminar talk at National Chung Cheng University, Department of Computer Science and Information Engineering, 2011 |
| **Immigration Status**: Green Card holder (Permanent Resident) |