國立臺灣師範大學九十五學年度碩士班考試入學招生試題

計算機系統 科試題（資訊工程研究所用，本試題共 6 頁）

注意：1.依次序作答，只要標明題號，不必抄題。
2.答案必須寫在答案卷上，否則不予計分。

1.

a) What is the decimal value of the following 32-bit two's complement number? (5 分)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0

b) What is the decimal value of the following IEEE 754 single-precision binary representation? (5 分)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2. Consider a five-stage (IF, ID, EX, MEM and WB) pipeline processor with hazard detection and data forwarding units. Assume the processor has instruction memory for IF stage, and data memory for MEM stage so that the structural hazard for memory references can be avoided.

a) Suppose the following code sequence is executed on the processor. Determine the average CPI (clock cycles per instruction) of the code sequence. (5 分)

```
ADD   R1, R2, R3;        R1 ← R2+R3
SUB   R4, R5, R6;        R4 ← R5-R6
```

b) Repeat Part (a) for the following code sequence. (5 分)

```
ADD   R1, R2, R3;        R1 ← R2+R3
SUB   R4, R1, R6;        R4 ← R1-R6
```

c) Repeat Part (a) for the following code sequence. (5 分)

```
LD    R3, 10(R7)         R3 ← MEM[R7+10]
ADD   R1, R2, R3;        R1 ← R2+R3
SUB   R4, R1, R6;        R4 ← R1-R6
```


請翻頁繼續作答

3. Consider a five-stage (IF, ID, EX, MEM and WB) pipeline processor with instruction memory for IF stage and data memory for MEM stage. Suppose the following code sequence is executed on the processor.

LD	R2,100(R1);	R2 ← MEM[R1+100]
LD	R4,200(R3);	R4 ← MEM[R3+200]
ADD	R6,R2,R4;	R6 ← R2+R4
SUB	R8,R2,R4;	R8 ← R2-R4
SD	R6,120(R1);	MEM[R1+120] ← R6
SD	R8,120(R3);	MEM[R3+120] ← R8

a) Determine the total number of memory references. (5 分)

b) Determine the percentage of the memory references which are data references. (5 分)

4.

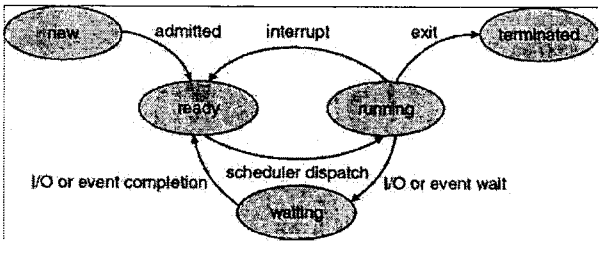
a) Consider a direct mapped cache with 64 blocks and a block size of 32 bytes. What block number does byte address 1600 map to? (5 分)

b) Repeat Part (a) for the byte address 3209. (5 分)

c) With a 32-bit virtual address, 8-KB pages, and 4 bytes per page table entry, determine the total page table size (in MB). (5 分)

5. In the following state diagram to the right (單選，3 分)

Event A: from ready state to running state
Event B: from running state to ready state
Event C: from running state to waiting state
Event D: from waiting state to ready state



Which events are preemptive?

a) BD
b) ABD
c) BC
d) AD
e) BCD

6. A process control block (PCB) contains necessary information of a process. Which item is usually not part of a PCB? (單選，3 分)

a) process state
b) registers
c) program counter
d) valid bits
e) list of open files

7. Given the following statement about DMA, (單選，3 分)

i. DMA is direct memory access

ii. When DMA is transferring data between I/O device and memory, the data does not go to registers in CPU.

iii. DMA is one kind of programmed I/O

iv. When the DMA controller seizes the memory bus, the CPU is momentarily prevented from accessing main memory.

v. DMA can slow down CPU computation, but generally improve the total system performance.

Which of the above statements are true?

a) i, iv, v
b) i, iii, v
c) i, ii, iv, v
d) i, ii, iii, iv
e) i, iii, iv, v

8. Fill in the blanks (填空，6 分)

- Modern operating system (O.S.) kernels provide a set of interfaces for user programs to request O.S. services. These interfaces are typically called 8(a).
- The interfaces of Windows are called 8(b).
- When a call to these interfaces is made, mode switch occurs to give user program privilege to execute kernel code. Such mode switch is typically accomplished by 8(c) instruction.

請翻頁繼續作答

9. When an hardware interrupt occurs, (3 分)

A. Jump to the address in the vector table
B. CPU saves the instruction pointer
C. fetch the address in the interrupt vector table
D. CPU saves the status register
E. Execute a return from interrupt instruction
F. Execute the body of interrupt handler

What is the correct order of the above steps: _____.

10. Suppose that a scheduling algorithm (at the level of short-term CPU scheduling) favors those processes that have used the least processor time in the recent past. In this scheduling strategy, (單選，4 分)

a) CPU bound programs are favored and I/O bound programs may be starved permanently.
b) I/O bound programs are favored but CPU bound programs may be starved permanently.
c) CPU bound programs are favored but I/O bound programs are not permanently starved
d) I/O bound programs are favored but CPU-bound are not permanently starved

11. Since each process cannot access other process's address space, how does O.S. support two processes to communicate and share data? (單選，4 分)

i. By allowing user programs to request a shared memory
ii. By allowing user programs to copy and access data (via system calls) at some places in kernel address space.
iii. By allowing user programs to set the data segment registers to an absolute address
iv. By allowing user programs to save data in registers and pass it to other processes.
v. By allowing user programs to store data in heap and open the heap for accessing by other process.

Which of the above statements are true?

a) i
b) i, iii, v
c) i, ii, iv
d) i, ii
e) ii, iii, v

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12. Among the page replacement algorithms, Optimal, FIFO, LRU, and Second Chance: （填空，4分）

- ___12(a)___ suffers Belady's anomaly.
- ___12(b)___ is adopted by real O.S.
- ___12(c)___ does not exist.
- ___12(d)___ usually does not have the needed hardware support.

13. A hardware company designs a CPU with two-level paging virtual memory. The page size is 512 bytes. A page table size is equal to page size. Each page table entry occupies 2 bytes (16 bits). In the page table entry, there are two bits reserved for present bit and modified bit. All the remaining 14 bits can be used to store frame numbers. （各2分，共8分）

- How many bits is a logical address (virtual address)? ___13(a)___
- How many bits (maximum) a physical address can be? ___13(b)___
- What is the maximum size (in bytes) of physical memory can be installed on this machine. ___13(c)___
- A program with size 384KB is loaded into memory. What is the maximum number of page tables (in number of pages) should be allocated for the process. ___13(d)___

14. Consider the following page-reference string （各2分，共6分）

1 2 3 4 2 1 5 6 2 1 2 3 4 7 6 3 2 1

Assume there are only 3 frames available. All frames are initially empty, so each first unique page will cost one fault. How many page faults will be caused by the following page replacement algorithm?

- LRU replacement: ___14(a)___.
- CLOCK (Second chance) replacement: ___14(b)___.
- Optimal replacement: ___14(c)___.

請翻頁繼續作答

15. Which of the following pairs of relationship between the file system and its allocation method are correct? （複選，3 分）

A. Unix: linked allocation

B. Unix: indexed allocation

C. DOS: linked allocation

D. DOS: contiguous allocation

E. DOS: indexed allocation

16. Which of the following linking characteristics are correct? （複選，3 分）

A. dynamic linking: a routine is not loaded until it is called

B. dynamic linking: linking is postponed until execution time

C. dynamic linking: generally require help from O.S.

D. static linking: linking is completed at compilation time

E. static linking: usually produce smaller size program

F. dynamic loading: a routine is not loaded until it is called

G. dynamic loading: generally does not require O.S. support