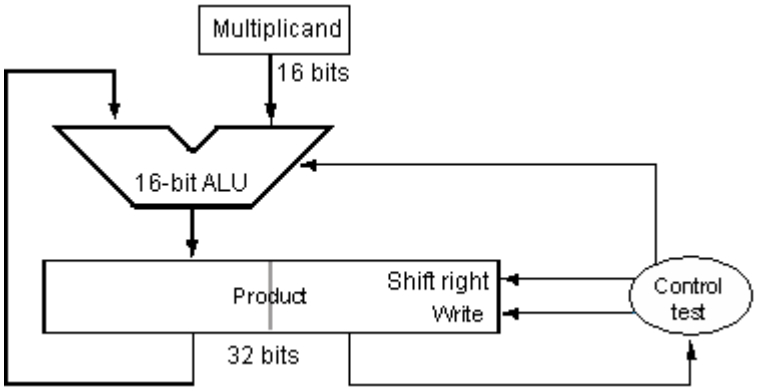
國立臺灣師範大學資訊工程學系
九十九學年度第二學期
博士班資格考

考試科目：計算機結構
總分一百分
請在答案卷作答，在題目卷上作答不予計分

1. (14pts) What are the decimal values of the following hexadecimal numbers, assuming they represent 2's complement integers?
   (a) (7pts) 0x12ab,
   (b) (7pts) 0xffffab12.

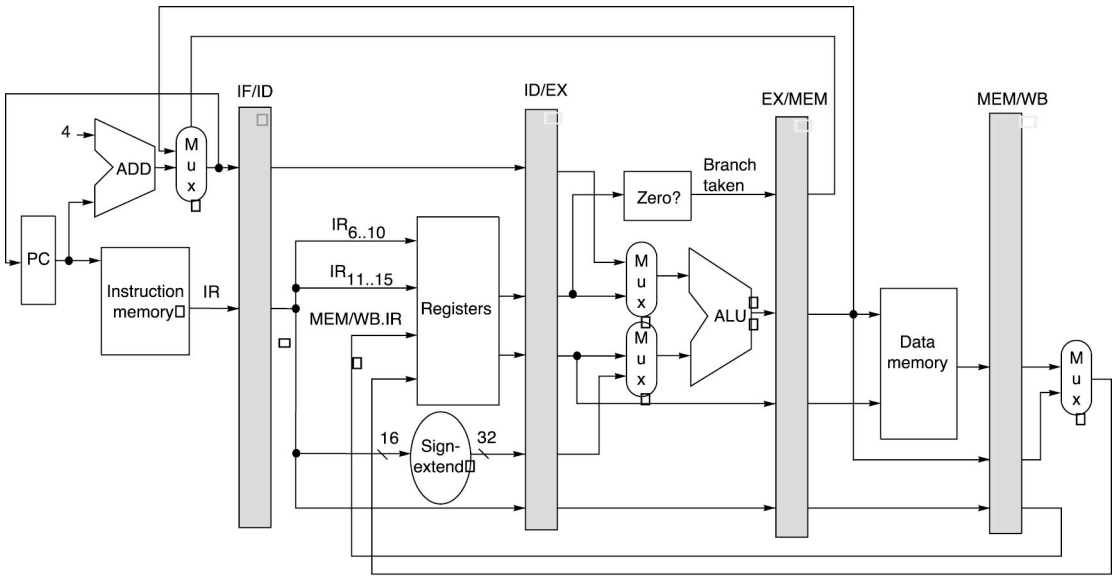
2. (16pts) A test program is executed on a processor P1 which has clock frequency 1GHz. One million instructions are executed and 2 milliseconds are needed.
   (a) (8pts) What is the CPI?
   (b) (8pts) Another processor (P2) is two times faster than P1, but has 1.1 times the CPI of P1. What is the clock frequency of P2?

3. (a) (10pts) Explain how a 16-bit multiplication is performed on the hardware shown below.



   (b) (10pts) Assume there is no multiplication instruction. Use MIPS instructions to implement the multiplication algorithm. Instructions you can use are *add, sub, addi, and, or, nor, andi, ori, sll, srl, beq*, *bne*, *slt, j*, and *jal*.

4. (20pts) Consider the simple 5-stage pipeline with forwarding and interlock as shown below.



Assume the pipeline is used for the execution of the following code sequence.

```
LD      R1,10(R2);
LD      R3,14(R2);
SUB     R5,R3,R1;
ADD     R6,R5,R3;
SD      R6,18(R2);
```

(a) (10pts) Suppose there is no cache miss for the execution. Show the timing of the code sequence. Your answer can be of the following form

Instruction		Clock Cycle																			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
LD	R1,10(R2);	IF	ID	EX	MEM	WB															
LD	R3,14(R2);																				
SUB	R5,R3,R1;																				
ADD	R6,R5,R3;																				
SD	R6,18(R2);																				

(b) (5pts) Determine the total number of memory accesses of the code sequence.

(c) (5pts) Assume the clock cycle time is 1 ns. Compute the CPU time when there is no cache miss. (in ns)

5. (15pts) Assume we have a computer where the CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2 % for instruction and data accesses, how much faster would the computer be if all memory accesses were cache hits?

6. (15pts) Briefly explain the following terms.
   (a) (3pts) Structural Hazards,
   (b) (3pts) Control Hazards,
   (c) (3pts) Direct mapped cache,
   (d) (3pts) N-way set associative cache,
   (e) (3pts) Translation lookaside buffer.